In the Claims:

1. (Original) An integrated circuit device, comprising:

a first-in first-out (FIFO) memory chip configured to support a pair of hybrid operating modes that enable the FIFO memory chip to be depth-expandable with other FIFO memory chips in a collective standard mode of operation, said pair of hybrid operating modes including a first hybrid mode that supports a write interface configured in standard mode and a read interface configured in first-word fall-through (FWFT) mode and a second hybrid mode that supports a write interface configured in FWFT mode and a read interface configured in standard mode.

2. (Original) The device of Claim 1, wherein the first hybrid mode supports a write interface having a full flag pin that designates when said FIFO memory chip is full and a read interface having an output ready pin that designates when said FIFO memory chip has at least one entry therein.

3. (Original) The device of Claim 2, wherein the second hybrid mode supports a write interface having an input ready pin that designates when said FIFO memory chip can accept additional entries and a read interface having an empty flag pin that designates when said FIFO memory chip is empty.

4. (Original) The device of Claim 3, wherein said FIFO memory chip has a pin that is responsive to a standard depth expansion mode signal.

5. (Original) The device of Claim 1, wherein said FIFO memory chip comprises a FIFO memory controller chip having cache memory arrays therein and a external memory interface that supports read and write data transfers between the cache memory arrays and a random access memory device.

6. (Original) The device of Claim 1, wherein said FIFO memory chip comprises:

a first cache memory device having a first page of quad-port memory cells therein that is configured to support writing and reading of FIFO vectors to and from columns in the first page and writing and reading of memory vectors to and from rows in the first page.

7. (Original) An integrated circuit system, comprising:

a plurality of first-in first-out (FIFO) memory controller chips that collectively support standard mode operation when cascaded in a depth expansion configuration.

8. (Original) The integrated circuit system of Claim 7, wherein said plurality of first-in first-out (FIFO) memory controller chips comprise a front-end FIFO memory controller chip disposed in a first hybrid mode that supports a corresponding write interface configured in standard mode and a corresponding read interface configured in first-word fall-through (FWFT) mode, and a back-end FIFO memory controller chip disposed in a second hybrid mode that supports a corresponding write interface configured in FWFT mode and a corresponding read interface configured in standard mode.

9. (Original) An integrated circuit device, comprising:

a first-in first-out (FIFO) memory chip having cache and embedded memory elements therein, said FIFO memory chip configured to support a pair of hybrid operating modes that enable said FIFO memory chip to be depth-expandable with other FIFO memory chips in a collective standard mode of operation, said pair of hybrid operating modes including a first hybrid mode that supports a write interface configured in standard mode and a read interface configured in first-word fall-through (FWFT) mode and a second hybrid mode that supports a write interface configured in FWFT mode and a read interface configured in standard mode.

10. (Original) The device of Claim 9, wherein the first hybrid mode supports a write interface having a full flag pin that designates when said FIFO memory chip is full and a read interface having an output ready pin that designates when said FIFO memory chip has at least one entry therein.

11. (Original) The device of Claim 10, wherein the second hybrid mode supports a write interface having an input ready pin that designates when said FIFO memory chip can accept additional entries and a read interface having an empty flag pin that designates when said FIFO memory chip is empty.

12. (Original) The device of Claim 11, wherein said FIFO memory chip has a pin that is responsive to a standard depth expansion mode signal.

13. (Original) An integrated circuit device, comprising:

a first-in first-out (FIFO) memory chip configured to support at least one hybrid operating mode that enables said FIFO memory chip to be depth-expandable with another FIFO memory chip in a collective standard mode of operation, said at least one hybrid mode supporting a write interface configured in standard mode and a read interface configured in first-word fall-through (FWFT) mode.